

# Optical Interconnect Solution With Plasmonic Modulator and Ge Photodetector Array

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**Abstract**—We report on an optical chip-to-chip interconnect solution, thereby demonstrating plasmonics as a solution for ultra-dense, high-speed short-reach communications. The interconnect comprises a densely integrated plasmonic Mach-Zehnder modulator array that is packaged with standard driving electronics. On the receiver side, a germanium photodetector array is integrated with trans-impedance amplifiers. A multicore fiber provides a compact optical interface to the array. We demonstrate  $4 \times 20$  Gb/s on-off keying signaling with direct detection.

**Index Terms**—Electrooptic modulators, multicore fiber, optical interconnects, photodetectors, plasmonics.

## I. INTRODUCTION

OPTICAL interconnects provide the high throughput and parallelism needed to cope with the continuously increasing bandwidth requirements in modern data centers [1]. The challenge though is to find a transmitter (Tx) and receiver (Rx) technology that can deliver ultra-fast communications on the most compact footprint without suffering from crosstalk. In addition, short-reach interconnects inside the datacenter (typical reach up to 2 km) should be technically simple and operate with conventional electronic drivers in an on-off keying (OOK) modulation format.

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Transceivers for optical interconnects are implemented either with separate chips for optical and electrical devices, referred to as heterogeneous integration or alternatively, with optical and electrical devices sharing the same chip, called monolithic integration [2]. Current transceivers mostly encompass heterogeneous integration which has the advantage of an optimized fabrication process for best optical and electrical device performance [3]–[5]. However, this strategy comes at the price of complicated packaging, limited density and higher interconnect parasitic capacitance. Monolithic integration can mitigate these issues. [2], [6]–[8]. Yet, the biggest challenge so far remains the integration of the Tx – and in particular the modulator. Unless integrated into resonant structures, the footprint of state-of-the-art modulators are far too large compared to their electronic counterparts [1]. However, resonant structures only operate at selected wavelengths and thus require sophisticated wavelength tuning. Highly integrated Mach-Zehnder modulators (MZMs) that offer operation across a large optical bandwidth remain a research topic to this day. Lately, Tx solutions based on plasmonics have emerged [9]. The most attractive feature of plasmonics is the ability to confine light below the diffraction limit. Thus, the size of electro-optic devices shrinks by orders of magnitude. Only recently, we have demonstrated high speed modulators in a plasmonic Mach-Zehnder configuration with line rates up to 108 Gbit/s at micrometer size [10], [11]. On the Rx side, compact solutions have indeed been demonstrated; e.g. based on germanium (Ge) photodetectors (PD) [12]. Another challenge towards a dense integration is a fiber-to-chip interface. In this respect, multicore fibers (MCF) have been proposed, offering both a small channel spacing and transmission over long distances [13], [14].

In this letter, we report on the first chip-to-chip interconnect bringing together the three components: a compact plasmonic Tx, a Germanium Rx and an MCF as a fiber-to-chip interface. The Tx comprises a plasmonic MZM array with its RF driving electronics. The size of the MZM array with  $20 \mu\text{m}$  long phase shifters is only dictated by the size of the electrical contact pads. Light from an external laser source is fed to the Tx via an MCF providing a channel spacing of only  $50 \mu\text{m}$ . The Rx consists of a Ge PD array integrated with trans-impedance amplifiers (TIAs). Finally, we show interconnect operation at  $4 \times 20$  Gbit/s with OOK signaling. The letter shows that plasmonics is a feasible path towards an ultra-compact, high-speed and technically simple interconnect.

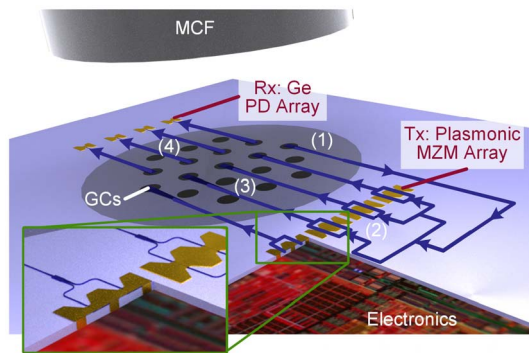


Fig. 1. Compact high-speed optical interconnect scenario: Integrated transceiver consisting of a plasmonic MZM array and a Ge photodiode array. For the Tx, (1) CW light of a central laser is coupled to the chip by a multicore fiber (MCF) matched to on-chip grating couplers (GCs). (2) The light is then distributed to the integrated plasmonic MZMs to encode a parallel data stream. (3) After encoding, the signals are sent back and fed into separate cores of the MCF. On the Rx side, (4) Ge PDs receive the signals stemming from different cores of the MCF. The electronic contacts of the devices may be realized through vias from the bottom of the chip as indicated in the magnified image.

## II. VISION

The interconnect solution envisioned here is shown in Fig 1. The highly dense transceiver is based on separate optical and electrical layers. The top optical layer consists of an optical interface and the active components, i.e. a plasmonic MZM array (Tx) and a Ge PD array (Rx). The optical interface comprises an array of grating couplers (GCs) matched to the cores of the MCF. The active components are driven individually by the underlying electronics. Metallic vias are used to bridge both layers as shown in the inset.

## III. TRANSMITTER

Towards the goal of a transceiver as shown in Fig 1, we built a prototype plasmonic Tx, see Fig. 2(a). A customized housing was fabricated in-house to assemble the photonic chip with the plasmonic MZM array and its driving electronics via wire bonding. The data signals were fed to the Tx via high-speed RF connectors at the edge of the housing. The driving RF signals were amplified by four RF amplifiers (Amp) mounted on an evaluation board that was designed and built in-house as well. To minimize the length of the wire bonds, the plasmonic MZM array was placed in a cavity in the middle of the housing, which provides two RF signals from each side. The housing was mounted on a copper block that acted both as an external heat sink to dissipate the heat from the RF amplifiers, and also to adjust the height of the sample to our characterization setup. No active cooling was required to operate the Tx. Light was coupled in and out of the photonic chip via silicon grating couplers (GCs) matched to an MCF and a standard single mode fiber (SMF), respectively. III2(b) shows the facet of the MCF with a  $50\ \mu\text{m}$  channel spacing in a hexagonal lattice of which only four cores were used in this work.

The plasmonic modulator array is shown in III2(c). It con-

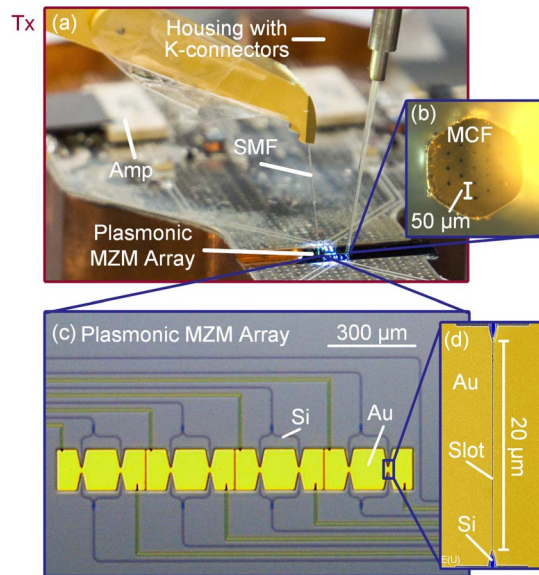


Fig. 2. Plasmonic transmitter (Tx). (a) Customized package with plasmonic modulator array on a photonic chip connected to its driving electronics via wire bonding. (b) Optical microscopy image of the facet of the MCF with a channel spacing of only  $50\ \mu\text{m}$ . (c) Four-channel plasmonic modulator array with silicon (Si) photonic Mach-Zehnder interferometers. The Si waveguides have vertical grating couplers at each end that match spacing and mode field size of the MCF. (d) Colorized scanning electron microscopy image of a plasmonic phase shifter consisting of two gold (Au) electrodes being separated by a  $75\ \text{nm}$  wide and  $20\ \mu\text{m}$  long slot that is filled with an organic second-order nonlinear optical material.

arranged in an imbalanced silicon Mach-Zehnder interferometer configuration. The chip was fabricated in-house, see [14]. The spacing between adjacent MZMs of  $300\ \mu\text{m}$  is given by the large size of the electrical contact pads required for wire bonding. Ultimately, these pads will not be needed in a monolithic integration concept. This way, the modulators may be contacted through vias from the bottom, so that smallest footprints will become possible. It should be noted, that we have already previously shown that multiple plasmonic MZMs can be arranged as close as a few  $\mu\text{m}$  without disturbing the device performance [15]. Further, while gold is not included in the CMOS process, it has been shown that it may be replaced by e.g. copper [16]. Once photonics is monolithically integrated with electronics, we expect lowest parasitics, thus taking full advantage of the ultra-compact plasmonic phase modulators.

The driving electronics were tested independently of the plasmonic modulators before wire bonding by using RF probes. Measurements of the S-parameters showed that the amplifiers provided  $>20\ \text{dB}$  gain up to  $10\ \text{GHz}$ , while the input reflection was better than  $-6\ \text{dB}$  up to  $40\ \text{GHz}$ . Data experiments at  $20\ \text{Gbit/s}$  resulted in open eye diagrams for all amplifiers, see Fig. 3. The test signal was a non-return-to-zero (NRZ) signal (pulse shape square-root-raised cosine SRRC, roll off  $\alpha = 0.35$ , De Bruijn bit sequences (DBBS), length  $2^{15}$ , input voltage  $V_{\text{pp}} = 500\ \text{mV}$ ). A digital sampling oscilloscope (DSO) was used to measure the quality factors  $Q^2$  of  $14.4\ \text{dB}$ ,  $14.1\ \text{dB}$ ,  $14.4\ \text{dB}$ , and  $11.8\ \text{dB}$  for

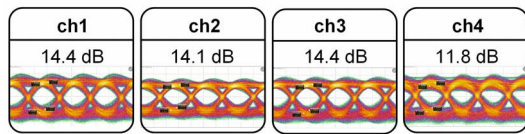


Fig. 3. Eye diagrams and quality factors  $Q^2$  at 20 Gbit/s for the four amplifiers before bonding to the plasmonic modulators. The eye amplitudes were 2.9 V, 2.9 V, 3.3 V, 3.3 V for ch1...4.

The plasmonic modulator array was also individually characterized using RF probes. We demonstrated  $4 \times 36$  Gbit/s in a coherent detection scheme with an optical interchannel crosstalk below  $-31$  dB as described in detail in [14]. In this work, the optical extinction ratios of the four imbalanced interferometers were found to be  $>11$  dB. The insertion loss of the plasmonic modulators on chip were  $\sim 18 \dots 21.6$  dB. Cut-back measurements of the silicon photonic devices indicate fiber-to-chip coupling losses and propagation losses of 8 dB per grating and 10 dB/cm, respectively, thus adding  $\sim 20$  dB to the loss budget. Assuming that for a single charging process the energy dissipated in the modulator is  $CV^2/2$  and that charging and discharging occurs statistically every second bit [17], [18], the estimated energy consumption of the modulator is  $w_{\text{bit}} = C_d U^2 / 4 = 327$  fJ/bit. Here, we used a driving voltage of  $U = \pm 3.3$  V and a capacitance of  $C_d = 30$  fF that was determined via reflectio coefficient measurements for a similar device on the same chip.

While the plasmonic modulators feature an electro-optic bandwidth  $>70$  GHz [14], [19], the electrical wire bonds with lengths of  $\sim 2.5$  mm introduce an electrical bandwidth limitation at higher data rates and should be minimized in future experiments.

#### IV. RECEIVER

The receiver consist of an integrated photodetector array packaged with trans-impedance limiting amplifie s (TIAs) on an evaluation board, see Fig. 4. The PD array consists of four Germanium waveguide photodetectors from IMEC's fully integrated silicon photonics platform [12]. The PDs feature a  $50 \mu\text{m}$  spaced optical interface with GCs and responsivities of  $0.5 \dots 0.65$  A/W with a bandwidth  $>22$  GHz. The detectors were wire bonded to a 4-channel TIA array on an evaluation board. To minimize the length of the wire bonds, the photonic chip was diced close to the contact pads and placed in proximity to the electronic chip. Note that one channel could not be operated, since one wire-bond detached from the pad.

We tested the performance of the Rx with data experiments, as shown in Fig 5. Data was encoded on an optical carrier by a GaAs intensity modulator (20 Gbit/s, NRZ, rectangular, DBBS 15,  $\lambda = 1550$  nm). The signal was used to characterize the three operational channels of the Rx sequentially. The modulated light was coupled to the individual channels using an SMF and GCs. The signal quality was evaluated using a DSO. A bias voltage of  $-2$  V was applied to the Ge PDs, while the Rx settings were optimized for high quality factors  $Q^2$  of the received eye diagrams. Fig 5 depicts open optical eye diagrams

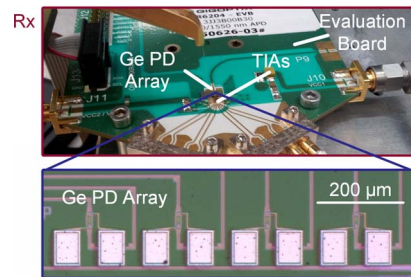


Fig. 4. Receiver (Rx). Evaluation board with Ge PD array wire-bonded to TIAs. The inset shows the four-channel Ge PD array with an electrical channels spacing of  $200 \mu\text{m}$ . One channel could not be operated due to a faulty wire bond.

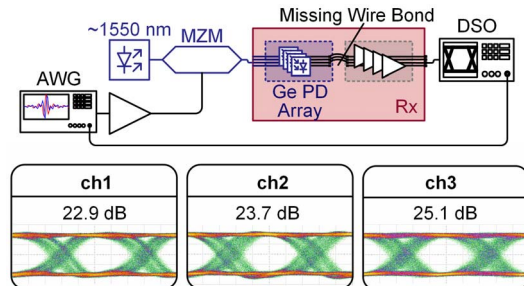


Fig. 5. Measurement setup and Rx optical eye diagrams with quality factor ( $Q^2$ ) of data experiments at 20 Gbit/s for -1 dBm input power.

and quality factors  $Q^2$  of 22.9 dB, 23.7 dB, and 25.1 dB of the investigated channels.

#### V. CHIP-TO-CHIP INTERCONNECT

In a fñal step, transmitter and receiver were combined to a complete chip-to-chip interconnect based on the setup shown in Fig 6. The Tx was operated at a wavelength of  $\sim 1550$  nm. Non-return-to-zero (NRZ) signals at 10 Gbit/s and 20 Gbit/s with a rectangular pulse shape and a DBBS with a pattern length of  $2^{15}$  were encoded on the optical carrier. The modulated signal was amplified by EDFAs before it was sent to the Rx. At the Rx output, the signals were measured with a real-time oscilloscope. Eye diagrams and bit error ratios (BERs) were obtained by standard digital signal processing. Each optical channel (ch1... 4) was tested separately. As already mentioned in the previous section, one channel of the Rx could not be addressed due to a missing wire bond. For this channel (ch4), an external photodiode without TIA was used instead. The power dissipation of one channel at the transmitter is  $\sim 1.4$  W, while the receiver contributes with  $\sim 240$  mW per channel. Fig. 7 depicts the measured BERs (40 million recorded bits) along with sample eye diagrams. The eye diagrams were digitally interpolated. Note that the eye diagram of ch4 looks different from the others due to the missing TIA. At 10 Gbit/s (20 Gbit/s) we achieved BERs of  $1.1 \times 10^{-6}$ ,  $< 2.5 \times 10^{-7}$ ,  $< 2.5 \times 10^{-7}$  and  $1.9 \times 10^{-5}$  ( $1.8 \times 10^{-3}$ ,  $6.3 \times 10^{-3}$ ,  $2.0 \times 10^{-4}$ ,  $1.8 \times 10^{-4}$ ) for ch1... 4. All channels have bit error ratios (BERs) below the FEC limit of  $7.0 \times 10^{-3}$  (9.1 % overhead) [20]. The BERs can be improved in the future by minimizing the



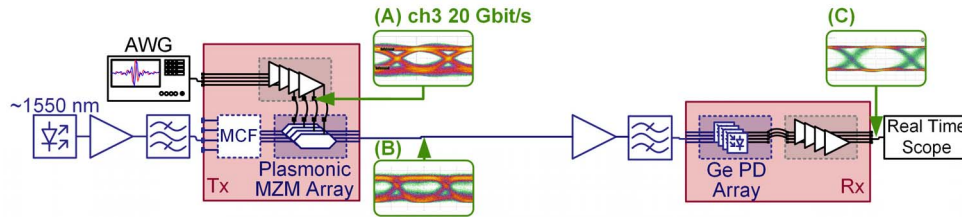


Fig. 6. Experimental setup for data modulation experiments of the complete chip-to-chip interconnect. Laser light at  $\lambda \approx 1550$  nm was coupled to the Tx. Electrical data streams were generated by an arbitrary waveform generator (AWG) and sent to the channel under test of the Tx. The modulated signal was amplified and sent to the Rx. At the Rx output, eye diagrams and bit error ratios were measured with a real time scope and standard digital signal processing. In green, exemplary eye diagrams of 20 Gbit/s signals measured with a DSO for channel 3: (A) Electrical signal after modulator drivers, (B) Optical signal leaving the Tx array measured with an external PD and (C) Signal at the output of the Rx.

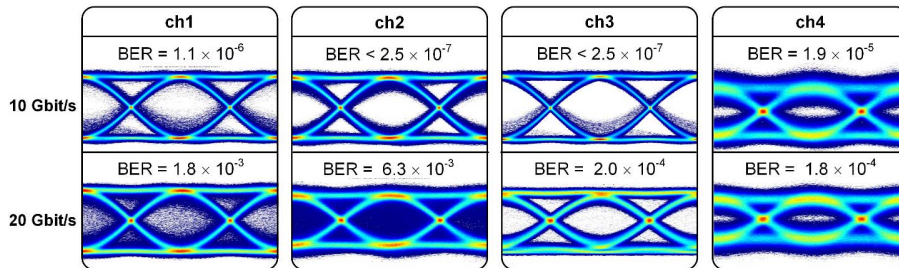


Fig. 7. NRZ OOK at 10 and 20 Gbit/s for all channels. Note, for ch4 an external photodiode without TIAs was used, since one wire bond on the Rx was missing.

insertion loss of the modulator that is attributed to fabrication imperfections.

## VI. CONCLUSION

A new chip-to-chip interconnect concept operating at  $4 \times 20$  Gbit/s (OOK) is introduced. The transmitter consists of an integrated plasmonic MZM array that is operated with standard driving electronics. Light is coupled to the array via an MCF with  $50 \mu\text{m}$  core spacing. The receiver comprises a Ge PD array packaged with TIAs. In conclusion, plasmonics is demonstrated as a compact, high-speed and scalable solution for short-reach interconnects.

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